FORM PTO-1449 SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1778.0180000	APPLICATION NO. 09/925,314
	FIRST NAMED INVENTOR Christopher R. Risucci	
	FILING DATE August 10, 2001	ART UNIT 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	3,794,980	02/1974	Cogar *et al.*			
	AB1	3,811,114	05/1974	Lemay *et al.*			
	AC1	3,840,861	10/1974	Amdahl *et al.*			
	AD1	3,983,541	09/1976	Faber *et al.*			
	AE1	4,110,822	08/1978	Porter *et al.*			
	AF1	4,149,244	04/1979	Anderson *et al.*			
	AG1	4,229,790	10/1980	Gilliland *et al.*			
	AH1	4,295,193	10/1981	Pomerene, James H.			
	AI1	4,432,056	02/1984	Aimura, Harutsugu			
	AJ1	4,467,409	08/1984	Potash *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK1	EP 0 073 424 A2	03/1983	Europe			N/A
	AL1	EP 0 239 081 B1	09/1995	Europe			N/A
	AM1	EP 0 368 332 B1	09/1997	Europe			N/A

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN1	Cobb, Paul, "TinyRISC: a MIPS-16 embedded CPU core," Presentation for Microprocessor Forum, 13 slides (7 pages) (October 22-23, 1996).
	AO1	U.S. Utility Patent Application No. 09/702,112, inventors Jensen, M., *et al.*, filed October 30, 2000 (not published) (67 pages).
	AP1	U.S. Utility Patent Application No. 09/702,115, inventors Jensen, M., *et al.*, filed October 30, 2000 (not published) (71 pages).
	AQ1	U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (9 pages).
	AR1	Preliminary Amendment, filed February 1, 2002, in U.S. Reissue Patent Application No. 10/066,475, inventor Edward Colles Nevill, filed February 1, 2002 (based on U.S. Pat. No. 6,021,265, issued February 1, 2000) (15 pages).

EXAMINER	DATE CONSIDERED
	8/12/05

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SECOND SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1778.0180000	09/925,314
FIRST NAMED INVENTOR	
Christopher R. Risucci	
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August 10, 2001	2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	4,507,728	03/1985	Sakamoto *et al.*			
	AB2	4,685,080	08/1987	Rhodes, Jr. *et al.*			
	AC2	4,724,517	02/1988	May, Michael D.			
	AD2	4,777,594	10/1988	Jones *et al.*			
	AE2	4,782,441	11/1988	Inagami *et al.*			
	AF2	5,132,898	07/1992	Sakamura *et al.*			
	AG2	5,241,636	08/1993	Kohn, Leslie D.			
	AH2	5,327,566	07/1994	Forsyth, Mark A.			
	AI2	5,355,460	10/1994	Eickemeyer *et al.*			
	AJ2	5,506,974	04/1996	Church *et al.*			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK2	EP 0 449 661 B1	11/1995	Europe			N/A
	AL2						Yes No
	AM2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN2	Gwennap, Linley, "VLIW: The Wave of the Future?: Processor Design Style Could Be Faster, Cheaper Than RISC," *Microprocessor Report*, Vol. 8, No. 2, pp. 18-21 (February 14, 1994).
	AO2	Kurosawa, K., *et al.*, "Instruction Architecture For A High Performance Integrated Prolog Processor IPP," *Logic Programming: Proceedings of the Fifth International Conference and Symposium (August 15-19, 1988)*, MIT Press, Cambridge, MA, Vol. 2, pp. 1506-1530 (1988).
	AP2	IBM Technical Disclosure Bulletin, "Patchable Read-Only Storage and Other Patchable Functions," Vol. 27, Issue 6, pp. 3496-3499 (November 1, 1984) (4 pages).
	AQ2	IBM Technical Disclosure Bulletin, "Patch RAM Load Technique," Vol. 27, Issue 6, pp. 3597-3598 (November 1, 1984) (3 pages).
	AR2	IBM Technical Disclosure Bulletin, "Microcode Memory Changes," Vol. 21, Issue 1, pp. 341-342 (June 1, 1978) (3 pages).

EXAMINER	DATE CONSIDERED
	9/12/05

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3	5,574,873	11/1996	Davidian, Gary G.			
	AB3	5,732,234	03/1998	Vassiliadis *et al.*			
	AC3	6,266,765 B1	07/2001	Horst, Robert W.			
	AD3	6,272,620 B1	08/2001	Kawasaki *et al.*			
	AE3	2001/0021970 A1	09/2001	Hotta *et al.*			
	AF3	2004/0054872 A1	03/2004	Nguyen *et al.*			
	AG3						
	AH3						
	AI3						
	AJ3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AK3						Yes No
	AL3						Yes No
	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN3	NEC Data Sheet, MOS Integrated Circuit, uPD30121, VR4121 64-/32-Bit Microprocessor (Copyright NEC Electronics Corporation 2000) (76 pages).
	AO3	Ross, Roger, "There's no risk in the future for RISC," *Computer Design*, Vol. 28, No. 22, pp. 73-75 (November 13, 1989).
	AP3	NEC User's Manual, VR4100 Series™, 64-/32-Bit Microprocessor Architecture, pp. 1-11 and 54-83 (Chapter 3) (Copyright NEC Corporation 2002).
	AQ3	
	AR3	

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THIRD SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.	APPLICATION NO.
1778.0180000	09/925,314
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1						
	AB1						
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR1	Case, Brian, "ARM Architecture Offers High Code Density: Non-Traditional RISC Encodes Many Options in Each Instruction," *Microprocessor Report*, Vol. 5, No. 23, pgs. 11-14 (December 18, 1991).
	AS1	
	AT1	

EXAMINER [signature] DATE CONSIDERED 8/12/05

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